CLAIMS

What is claimed is:

1. A SONET multiplexed communications system, comprising:

pointer processing circuitry clocked by a first clock, the pointer processing circuitry being configured to process at least one SONET signal comprising data and overhead information;

at least one overhead information insertion circuit clocked by a second clock, the insertion circuit being configured to re-generate the overhead information and insert the re-generated overhead information in the SONET signal; and

at least one clock domain transfer circuit coupled between the pointer processing circuitry and the insertion circuit, the clock domain transfer circuit including at least one first buffer having a plurality of addressable locations configured to store the data and overhead information of the SONET signal,

wherein the clock domain transfer circuit is configured to compensate for timing differences between the first and second clocks by addressing the plurality of first buffer locations for selectively overwriting or skipping at least one location corresponding to the overhead information of the SONET signal.

2. The multiplexed communications system of claim 1 wherein the pointer processing circuitry includes a monitor circuit configured to determine which first

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buffer location corresponding to the data and overhead information of the SONET signal is being addressed by the clock domain transfer circuit.

3. The multiplexed communications system of claim 2 wherein the clock domain transfer circuit further includes a buffer fill calculation circuit clocked by the first clock and configured to determine whether the first buffer is nearly full or nearly empty upon receipt of an inquiry signal.

4. The multiplexed communications system of claim 3 wherein the monitor circuit is further configured to send the inquiry signal to the buffer fill calculation circuit in the event it is determined that the first buffer location corresponding to the overhead information is being addressed by the clock domain transfer circuit.

5. The multiplexed communications system of claim 3 wherein the buffer fill calculation circuit is further configured to cause the clock domain transfer circuit to address the plurality of first buffer locations for overwriting at least one location corresponding to the overhead information in the event the first buffer is determined to be nearly full.

6. The multiplexed communications system of claim 3 wherein the buffer full calculation circuit is further configured to cause the clock domain transfer circuit to address the plurality of first buffer locations for

skipping at least one location corresponding to the overhead information in the event the first buffer is determined to be nearly empty.

7. The SONET multiplexed communications system of claim 2 wherein the SONET signal comprises at least one multi-byte frame and the overhead information re-generated by the overhead information insertion circuit includes a frame start indicator for the multi-byte frame, the monitor circuit being further configured to use the frame start indicator for determining which first buffer location corresponding to the data and overhead information of the SONET signal is being addressed by the clock domain transfer circuit.

8. The SONET multiplexed communications system of claim 7 wherein the clock domain transfer circuit further includes at least one second buffer having a plurality of addressable locations configured to receive the frame start indicator from the overhead information insertion circuit, store the frame start indicator, and provide the frame start indicator to the monitor circuit.

9. The SONET multiplexed communications system of claim 8 wherein the first buffer and the second buffer have the same depth.

10. The SONET multiplexed communications system of claim 3 wherein the monitor circuit includes a counter and an overhead information location circuit, the counter being

configured to provide a plurality of outputs representing at least row and column information for the SONET signal, the location circuit being configured to locate at least one first buffer location corresponding to the overhead information of the SONET signal.

11. The SONET multiplexed communications system of claim 1 wherein the pointer processing circuitry includes a single pointer interpreter, a single pointer generator, and a single first-in first-out buffer coupled between the pointer interpreter and the pointer generator, and the pointer processing circuitry is further configured to modify an extraction of data from the single first-in first-out buffer to account for the overwriting or skipping of at least one first buffer location corresponding to the overhead information of the SONET signal by the clock domain transfer circuit.

12. The SONET multiplexed communications system of claim 1 wherein the clock domain transfer circuit further includes a first counter clocked by the first clock and a second counter clocked by the second clock, the first buffer having at least one input clocked by the first counter and at least one output clocked by the second counter.

13. The SONET multiplexed communications system of claim 12 wherein the clock domain transfer circuit is configured to compensate for timing differences between the first and second clocks by selectively causing the

first counter to advance by two counts for a single cycle of the first clock in the event the first buffer is nearly empty or not advance for a single cycle of the first clock in the event the first buffer is nearly full.

14. The SONET multiplexed communications system of claim 11 wherein the single pointer interpreter comprises a plurality of logical pointer interpreters configured to process the respective SONET signals.

15. The SONET multiplexed communications system of claim 11 wherein the single first-in first-out buffer comprises a plurality of logical first-in first-out buffers configured to store the respective SONET signals.

16. A method of operating a SONET multiplexed communications system, comprising the steps of:

processing at least one SONET signal comprising data and overhead information by pointer processing circuitry clocked by a first clock;

storing the data and overhead information of the SONET signal by a respective first buffer disposed in at least one clock domain transfer circuit, the first buffer having a plurality of addressable locations;

compensating for timing differences between the first clock and a second clock by addressing the plurality of first buffer locations for selectively overwriting or skipping at least one location corresponding to the overhead information of the SONET signal by the clock domain transfer circuit; and

re-generating the overhead information and inserting the re-generated information in the SONET signal by at least one overhead information insertion circuit clocked by the second clock.

17. The method of claim 16 wherein the processing step includes processing a plurality of SONET signals comprising respective data and overhead information by the pointer processing circuitry, and the storing step includes storing the respective data and overhead information of the plurality of SONET signals by respective first buffers disposed in a plurality of clock domain transfer circuits.

18. The method of claim 17 wherein the processing step includes interpreting pointers of the respective SONET signals by a plurality of logical pointer interpreters included in the pointer processing circuitry.

19. The method of claim 17 wherein the processing step includes storing the respective SONET signals in a plurality of logical first-in first-out buffers included in the pointer processing circuitry.